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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,597	03/10/2004	Xiaobao Wang	015114-054911US	6353

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EXAMINER	
CHANG, DANIEL D	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 09/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,597	WANG ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-15* is/are allowed.

6)☒ Claim(s) *1,3,16-21 and 23* is/are rejected.

7)☒ Claim(s) *2,4,22 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/1/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(i) & 37 CFR 1.84(p) because lines, numbers & letters are not uniformly thick and well defined, clean, durable, and black (poor line quality). Also, some characters are too small.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 16-21, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Vishwanthaiah et al. (US 5,955,894, "Vishwanthaiah" hereinafter).

Regarding claim 1, Vishwanthaiah discloses, in Figs. 1-5, an integrated circuit (102a) comprising:

a first on-chip impedance termination circuit (212 in first driver circuit 110 in fig. 1; see col. 4, lines 9+) coupled to a first pad of the integrated circuit;

a second on-chip impedance termination circuit (222 in second driver circuit 110 in fig. 1; see col. 4, lines 9+) coupled to a second pad of the integrated circuit;

a first control circuit (302 in Fig. 3) that adjusts the impedance of the first on-chip impedance termination circuit; and

a second control circuit (304 in Fig. 3) that adjusts the impedance of the second on-chip impedance termination circuit independently of the impedance of the first on-chip impedance termination circuit.

Regarding claim 3, Vishwanthaiah discloses, in Figs. 1-5, an integrated circuit (102a) comprising:

a first on-chip impedance termination circuit (212 in first driver circuit 110 in fig. 1; see col. 4, lines 9+) coupled to a first pad of the integrated circuit;

a second on-chip impedance termination circuit (222 in second driver circuit 110 in fig. 1; see col. 4, lines 9+) coupled to a second pad of the integrated circuit;

a first control circuit (302 in Fig. 3) that receives a first signal (VDDO/2 with 122 or 120) indicative of an off-chip resistance and a second signal (310) that indicates an adjusted

impedance value for the first pad, the first control circuit adjusting the impedance of the first on-chip impedance termination circuit to a first impedance value in response to the first and the second signals; and

a second control circuit (304 in Fig. 3) that receives the first signal and a third signal (312) that indicates an adjusted impedance value for the second pad, the second control circuit adjusting the impedance of the second on-chip impedance termination circuit to a second impedance value in response to the first and the third signals.

Regarding claim 16, Vishwanthaiah discloses, in Figs. 1-5, a method for providing termination impedance to a pin on an integrated circuit, the method comprising:

generating digital signals (310, 312) in response to a signal indicative of an impedance of an off-chip resistor (120, 122);

shifting (406, 506) the digital signals by at least one bit to generate bit shifted signals (BIT1-BIT8 of 402); and

setting a total impedance of first transistors (204 in Fig. 2) using the bit shifted signals, the first transistors being coupled in parallel and to a first pin (inherent first pin connected to first driver 110 shown in Fig. 1) on the integrated circuit, each of the first transistors being coupled to receive one of the bit shifted signals.

Regarding claim 17, Vishwanthaiah discloses, in Figs. 1-5, that shifting the digital signals by at least one bit to generate the bit shifted signals further comprises shifting the digital signals to the right (RIGHT in 406, 506; col. 7, lines 33+) by one bit to increase the total impedance of the first transistors.

Regarding claim 18, Vishwanthaiah discloses, in Figs. 1-5, that shifting the digital signals by at least one bit to generate the bit shifted signals further comprises shifting the digital signals to the left (LEFT in 406, 506; col. 7, lines 33+) by one bit to decrease the total impedance of the first transistors.

Regarding claim 19, Vishwanthaiah discloses, in Figs. 1-5, that shifting the digital signals by at least one bit to generate second bit shifted signals (BIT1-BIT8 of 502); and

setting a total impedance of second transistors (202 in Fig. 2) using the second bit shifted signals, the second transistors being coupled in parallel, each of the second transistors being coupled to a second pin (inherent second pin connected to second driver 110 shown in Fig. 1) on the integrated circuit and to one of the second bit shifted signals.

Regarding claim 20, Vishwanthaiah discloses, in Figs. 1-5, that shifting the digital signals by at least one bit to generate the second bit shifted signals further comprises shifting the digital signals to the left (LEFT in 406, 506; col. 7, lines 33+) by one bit to decrease the total impedance of the second transistors.

Regarding claim 21, Vishwanthaiah discloses, in Figs. 1-5, that shifting the digital signals by at least one bit to generate bit shifted signals further comprises:

shifting the digital signals by two bits (by 406, 506; col. 7, lines 33+) to generate the bit shifted signals.

Regarding claim 23, Vishwanthaiah discloses, in Figs. 1-5, that the first transistors (see 204 in Fig. 2) are coupled to provide parallel termination impedance to the first pin; and the second transistors (see 202 in Fig. 2) are coupled to provide series termination impedance to the second pin.

Allowable Subject Matter

Claims 5-15 are allowable over the prior art.

Claims 2, 4, 22, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER